CLAIMS

What is claimed is:

1. An apparatus, comprising:

an integrated system management memory region; and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by a processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

2. The apparatus of claim 1, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

3. The apparatus of claim 2, wherein the system management interrupt address is the first address received following the assertion of the system management interrupt acknowledge signal by the processor.

4. The apparatus of claim 3, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

5. The apparatus of claim 4, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in a system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

6. The apparatus of claim 5, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

7. The apparatus of claim 6, wherein the integrated system management memory region is at least 128 bytes in size.

8. A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller in response to the system management interrupt acknowledge signal.

9. The method of claim 8, wherein fetching a plurality of system management interrupt handler instructions from an integrated system management memory includes fetching the system management interrupt handler instructions from the integrated system management memory regardless of a system management memory address indicated by the processor.

10. The method of claim 9, further comprising latching the system management memory address indicated by the processor.

11. The method of claim 10, wherein latching the system management memory address includes latching a first address delivered by the processor following receiving the system management interrupt acknowledge signal.

11 10
~~12~~. The method of claim ~~11~~, further comprising comparing a plurality of addresses received from the processor with the latched address.

12 11
~~13~~. The method of claim ~~12~~, further comprising fetching a plurality of system management interrupt handler instructions from a section of BIOS code in a system main memory if comparing a plurality of addresses received from the processor with the latched address results in a match.

13
~~14~~. A system, comprising:

a processor;

a system main memory; and

a memory controller coupled between the processor and the system main memory, the memory controller including

an integrated system management memory region, and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by the processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

14 13
~~15~~. The system of claim ~~14~~, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

15 14
~~16~~. The system of claim ~~15~~, wherein the system management interrupt address is the first address received by the memory controller following the assertion of the system management interrupt acknowledge signal by the processor.

16 15
~~17~~. The system of claim ~~16~~, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

17 16
~~18~~. The system of claim ~~17~~, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in the system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

19. The system of claim 18, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

19 18
~~20~~. The system of claim ~~19~~, wherein the integrated system management memory region is at least 128 bytes in size.